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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/006,334	12/03/2001	Kamesh V. Gadepally	NSC1-G0610 [P04402 P01]	3399

7590 10/23/2002

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EXAMINER
HOANG, QUOC DINH

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 10/23/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/006,334	GADEPALLY, KAMESH V.	
	Examiner	Art Unit	
	Quoc D Hoang	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement filed on 12/03/01 has been considered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-12 are rejected under 35 U.S.C 103(a) as being unpatentable over Hsu., (US Patent 6,087,227) in view of Goto et al., (US Pat 6,197,646).

Regarding claims 1 and 8, Hsu., Figs. 1-3, and related text on col. 1-7 which discloses a method for forming cobalt salicide regions and cobalt salicide exclusion regions during the manufacturing of an integrated circuit (IC), the method comprising the steps of (a) providing an IC structure including a plurality of MOS transistor structures, the plurality of MOS transistor structures having exposed silicon surfaces (col.6, lines 5-67 and Fig. 3A); (b) depositing a cobalt layer 430 on the IC structure in a controlled manner (col.6, lines 25-30 and Fig. 3B); (d) forming a photoresist masking layer 430 on those MOS transistor structures where cobalt salicide regions are to be formed (col.6, lines 30-35 and Fig. 3C); (e) removing the cobalt layer 430 from those MOS transistor structures where cobalt salicide exclusion regions are to be formed (col.6, lines 37-43 and Fig. 3D); (f) after step (e), stripping the photoresist masking layer 432 (col.6, lines 43-

65 and Fig. 3E); and (g) after step (f), reacting cobalt in the cobalt layer 430 with silicon 410 in the exposed silicon surfaces to form cobalt salicide regions 450 (col.7, lines 1-10 and Fig. 3F).

Hsu., does not disclose depositing a capping layer on the cobalt layer. Also, Hsu., does not disclose wherein step (b) includes the step of controlling at least one metal deposition parameter such that the cobalt layer has at least one predetermined property, and the at least one predetermined property is such that at least one of the cobalt salicide regions formed in step (g) has at least one predetermined attribute.

Goto et al., discloses in figure 6A and on columns 10-11 a step © depositing a capping layer on the cobalt layer (col. 11, lines 9-15), and wherein step (b) includes the step of controlling at least one metal deposition parameter such that the cobalt layer has at least one predetermined property, and the at least one predetermined property is such that at least one of the cobalt salicide regions formed in step (g) has at least one predetermined attribute (col. 10, lines 50-67 and Fig. 6A).

Hsu., and Goto et al., are combinable because they are from the same field of endeavor. At the time of the invention it would have been obvious to a person of ordinary skill in the art to control the refractory metal thickness formed on the silicon gate electrode. The motivation for doing so is to control the sheet resistance of the metal silicide layer.Therefore, it would have been obvious to combine Hsu., with Goto et al., to obtain the invention of claims 1 and 8.

Regarding claims 2 and 9, Goto et al., discloses one predetermined attribute of said at least one of the metal salicide regions is a sheet resistance (col. 10, lines 50-67 and Fig. 6A).

Regarding claims 3 and 10, Goto et al., discloses one predetermined attribute of said at least one of the cobalt salicide regions is a conductivity (col. 10, lines 50-67 and Fig. 6A).

Regarding claims 4 and 11, Goto et al., discloses at least one predetermined property of the cobalt layer is a thickness of said cobalt layer (col. 10, lines 50-67 and Fig. 6A).

Regarding claims 5 and 12, Goto et al., discloses the removal during step (e) of the cobalt layer from those MOS transistor structures where cobalt salicide exclusion regions are to be formed, is performed in a manner significantly limiting cobalt salicide crawl over and under the cobalt salicide regions formed during step (g) (col. 10, lines 50-67 and Fig. 6A).

Regarding claim 6, Goto et al., discloses the metal layer deposited in step (b) comprises metal selected from the group consisting of cobalt, titanium, tantalum, nickel and molybdenum (col. 10, lines 50-67 and Fig. 6A).

Regarding claim 7, Goto et al., discloses the metal layer deposited in step (b) has a thickness in the range of 150 to 500 angstroms (col. 11, lines 1-5 and Fig. 6A).

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quoc Hoang whose telephone number is (703) 306-5795. The examiner can normally be reached on Monday -Friday from 8.00 AM to 5.00 PM.

If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms., can be reached on (703) 308-4910

Quoc Hoang
Patent Examiner/ AU 2818

HOAI HO
PRIMARY EXAMINER